

VHDL Cheat-Sheet

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Concurrent Statements		Sequential Statements
Concurrent Signal Assignment <i>(dataflow models)</i>	⇐	Signal Assignment
target <- expression;		target <- expression;
A <- B AND C; DAT <- ED AND E3 OR (F AND G);		A <- B AND C; DAT <- ED AND E3 OR (F AND G);
Conditional Signal Assignment <i>(dataflow models)</i>	↔	if statements
target <- expression when condition else expression when condition else expression;		if (condition) then { sequence of statements } elsif (condition) then { sequence of statements } else --(the else is optional) { sequence of statements } end if;
F3 <- '1' when (L='0' AND H='0') else '1' when (L='1' AND H='1') else '0';		if (CSL = '111') then F_CTRL <= D472; elsif (CSL = '110') then F_CTRL <= D482; elsif (CSL = '101') then F_CTRL <= D412; elsif (CSL = '000') then F_CTRL <= D402; else F_CTRL <= '0'; end if;
Selective Signal Assignment <i>(dataflow models)</i>	⇐	case statements
with choice_expression select target <- expression when choice, expression when choice;		case expression is when choice => {sequential statements} when choice => {sequential statements} when others => -- (optional) {sequential statements} end case;
with ctrl select F_OUT <- D3 when '11', D2 when '10', D1 when '01', D0 when '00', '0' when others;		case ctrl is when '100' => F_OUT <= '1'; when '011' => F_OUT <= '1'; when '111' => F_OUT <= '1'; when others => F_OUT <= '0'; end case;
Process <i>(behavioral models)</i>		
opt_label: process (mode [, div [, sig [, list]]) begin {sequential statements} end process opt_label;		
proc1: process (A, B, C) begin if (a = '1' and b = '0') then r_out <= '1'; elsif (a = '1' and c = '1') then r_out <= '1'; else r_out <= '0'; end if; end process proc1;		

Guide To Vhdl Syntax A

Jiyuan Zhang



Guide To Vhdl Syntax A:

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Guide To Vhdl Syntax A Introduction

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